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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/631,897
Filing Date: August 01, 2003
Appellant(s): NAKAYAMA, MASAHIKO

Ian R. Blum
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 02/09/2006 appealing from the Office action mailed 11/13/2004.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

(9) Grounds of Rejection

Claim 5 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Christopher (4,731,851).

Christopher discloses in figure 6 a decibel level adjustment device including a plurality of signal lines (503, 504,506,508) arranged parallel to each other for producing in advance signals (vertical part of 503, and outputs from 504,506 and 508) that are shifted a number of bits necessary for operating on the input signal (the weighting circuits 504,506,508 as disclosed in col. 9, lines 12-14, are "hardwired bit shift arrangements" that is the output of an arrangement is the input being shifted by a number of bits). The device also has at least one switch means (510,512,514) for selecting outputs of the plurality of signal lines or all 0 (the gating 510,512,514 clearly provide the input as the output when enabled, or 0 as the output when disabled in order for the device to function properly). The device further includes a switch control circuit means (518,C0,C1) for receiving the a decibel control value and switching the switches in accordance with the decibel control value, and an adder circuit means (516) for adding together the outputs of the switches and output of the signal line (vertical part of 503) that does not pass by way of the switches as claimed.

(10) Response to Argument

It is disagreed with to appellant's argument that the reference does not disclose a plurality of signal lines arranged parallel to each other for producing in advance signals that are shifted a number of bits necessary for operating on said input signal. Figure 6 in Christopher clearly shows a plurality of signal lines arranged parallel to each other for producing in advance signals the are the vertical part of 503, and outputs from 504,506 and 508 that are shifted a number of bits necessary for operating on the input signal. It should be noted that a result of multiplying/ dividing an input (in binary) by a power of 2 equals to the input being shifted left/right by a number of bit equaling to the power (see the sentence bridging cols 8 and 9 of Christopher). The the weighting circuits 504,506,508 as disclosed in col. 9, lines 8-14, are to scale the signal 503 by powers of 2, and thus produce outputs that equal to the signal 503 being shifted by a numbers of bit. In particular, the output of 504 is the signal 503 being right shifted by 2 bit (divided by 4=2^2), the output of 506 is the signal 503 being right shifted by 4 bit (divided by 16=2^4), the output of 508 is the signal 503 being right shifted by 1 bit (divided by 2=2^1), and the signal 503 is the input signal 40 being shifted by a number of bits by the shifter 501. Therefore, the weighting circuits 504,506,508 are suggested to be "simple hardwired bit shift arrangements" that is the output of the arrangements is the input being shifted by a fixed number of bit.

Moreover, even if the reference is interpreted as explained by the appellant as in the brief, page 9, lines 11-16, the parallel signal lines in figure 6 would also meet the claimed limitation because claim 5 does not require each signal lines being shifted by a different number of bits, and in Christopher, each signal line is the input signal being shifted by a number of bits by at least the shifter 501.

It is also disagreed with to appellant's argument that there is no switch in Christopher with the function for selecting outputs of the plurality of lines or all "0". The gating elements 510,512,514 in figure 6 of Christopher clearly read on the claimed switching means since they are clearly to provide either signals in the parallel lines (when enabled), or otherwise zero (when disabled) to the adder 502 in accordance with control signals. A value other than zero if provided to the adder 502 by a gating element when disabled would clearly result in an incorrect and undesired result.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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